CLAIMS

No claims are amended, added, or canceled by this response. For the Examiner's convenience, a copy of all pending claims and a status of the claims is provided below.

1. (original) A method, comprising:

forming a pattern of strained material and relaxed material on a substrate;

forming a strained device in the strained material; and

forming a non-strained device in the relaxed material.

2. (original) The method of claim 1, wherein the step of forming a pattern of strained material and relaxed material on a substrate further comprises:

forming a recess in the substrate, the recess having sidewalls;

forming a buffer layer in the recess which has a lattice constant/structure mismatch with the substrate;

forming a relaxed layer on the buffer layer;

forming the strained material on the relaxed layer and the relaxed material on the substrate, wherein the relaxed layer has a lattice constant/structure mismatch with the strained material.

3. (original) The method of claim 2, further comprising forming an insulating layer on the sidewalls before forming the buffer layer.

4. (original) The method of claim 2 wherein the relaxed layer and the buffer layer are each selected from the group consisting of silicon carbon (SiC), silicon germanium (SiGe), $Al_{X1}Ga_{X2}In_{X3}As_{Y1}P_{Y2}N_{Y3}Sb_{Y4}$, where X1, X2, X3, Y1, Y2, Y3, and Y4 represent relative proportions, each greater than or equal to zero and X1+X2+X3+Y1+Y2+Y3+Y4=1 (1 being the total relative mole quantity), and $Zn_{A1}Cd_{A2}Se_{B1}Te_{B2}$, where A1, A2, B1, and B2 are relative proportions each greater than or equal to zero and A1+A2+B1+B2=1 (1 being a total mole quantity).

5. (original) The method of claim 2, wherein the strained material and the relaxed material are each selected from one of the group consisting of silicon (Si), silicon carbon (SiC), silicon germanium (SiGe), $Al_{X1}Ga_{X2}In_{X3}As_{Y1}P_{Y2}N_{Y3}Sb_{Y4}$, where X1, X2, X3, Y1, Y2, Y3, and Y4 represent relative proportions, each greater than or equal to zero and X1+X2+X3+Y1+Y2+Y3+Y4=1, and $Zn_{A1}Cd_{A2}Se_{B1}Te_{B2}$, where A1, A2, B1, and B2 are relative proportions each greater than or equal to zero and A1+A2+B1+B2=1.

6. (original) The method of claim 2, wherein the step of forming the buffer layer further comprises:

epitaxially growing multiple layers of a material forming the buffer layer such that the material forming the buffer layer has a base concentration proximate the substrate and an increased benchmark concentration proximate the relaxed layer.

7. (original) The method of claim 6, wherein the step of forming the relaxed layer further comprises:

epitaxially growing multiple layers of a material forming the relaxed layer such that the material forming the relaxed layer has a second base concentration proximate the buffer layer that approximately equals the bench-mark concentration of the buffer layer material.

8. (withdrawn) The method of claim 1, wherein the step of forming the pattern of strained material and relaxed material on the substrate further comprises:

forming a buffer layer on the substrate, the buffer layer having a lattice constant/structure mismatch with the substrate;

forming a relaxed layer on the buffer layer;

forming a recess through the relaxed layer and the buffer layer, the recess having sidewalls;

forming the relaxed material in the recess; and

forming the strained material on the relaxed layer outside the confines of the recess, the strained material having a lattice constant/structure mismatch with the relaxed layer.

9. (withdrawn) The method of claim 8, further comprises forming an insulating layer on the sidewalls before forming the relaxed layer in the recess.

10. (withdrawn) The method of claim 8, wherein the relaxed layer and the buffer layer are selected from the group consisting of silicon carbon (SiC), silicon germanium (SiGe), $Al_{X1}Ga_{X2}In_{X3}As_{Y1}P_{Y2}N_{Y3}Sb_{Y4}$, where X1, X2, X3, Y1, Y2, Y3, and Y4 represent relative proportions, each greater than or equal to zero and X1+X2+X3+Y1+Y2+Y3+Y4=1, and

$Zn_{A1}Cd_{A2}Se_{B1}Te_{B2}$, where A1, A2, B1, and B2 are relative proportions each greater than or equal to zero and A1+A2+B1+B2=1.

11. (withdrawn) The method of claim 8, wherein the step of forming the buffer layer further comprises epitaxially growing multiple layers of a material forming the buffer layer such that the material forming the buffer layer has a base concentration proximate the substrate and an increased bench-mark concentration proximate the relaxed layer.

12. (withdrawn) The method of claim 11, wherein the step of forming the relaxed layer further comprises epitaxially growing multiple layers of a material forming the relaxed layer such that the material forming the relaxed layer has a second base concentration proximate the buffer layer that approximately equals the benchmark concentration of the buffer layer material.

13. (original) The method of claim 1, wherein the strained material is formed of carbon-doped silicon or germanium doped silicon.

14. – 19. (canceled)

20. (original) The method of claim 1, wherein the strained material is a semiconductor material doped by carbon or germanium.

21. – 30. (canceled)

31. (original) An electrical device, comprising:

a pattern of strained material and relaxed material formed on a substrate;

a first device formed in the first strained material; and

a second device formed in the relaxed material.

32. (withdrawn) The electrical device of claim 31, further comprising:

a buffer layer formed in contact with a portion of a substrate, the buffer layer having a lattice constant/structure mismatch with the substrate;

a relaxed layer formed on the buffer layer;

a strained material formed on a top surface of the relaxed layer, wherein the relaxed layer places the strained material in one of a tensile or a compressive state; and

a non-strained material patterned proximate the strained material.

33. (withdrawn) The electrical device of claim 31, wherein the first device formed in the strained material is a logic device and the second device formed in the non-strained material is a defect-sensitive device.

34. (withdrawn) The electrical device of claim 32, wherein the relaxed material comprises a material which has a lattice constant/structure mismatch with the strained material.

35. (withdrawn) The electrical device of claim 32, wherein the buffer layer and the relaxed layer are selected from the group consisting of silicon carbon (SiC), silicon germanium (SiGe), $Al_{X1}Ga_{X2}In_{X3}As_{Y1}P_{Y2}N_{Y3}Sb_{Y4}$, where X1, X2, X3, Y1, Y2, Y3, and Y4 represent relative

proportions, each greater than or equal to zero and X1+X2+X3+Y1+Y2+Y3+Y4=1, and $Zn_{A1}Cd_{A2}Se_{B1}Te_{B2}$, where A1, A2, B1, and B2 are relative proportions each greater than or equal to zero and A1+A2+B1+B2=1.

36. (withdrawn) The electrical device of claim 32, wherein a material forming the buffer layer increases in concentration from a base concentration proximate the substrate to a benchmark concentration proximate the relaxed layer.

37. (withdrawn) The electrical device of claim 32, wherein the strained material is a carbon doped semiconductor material or a germanium doped semiconductor material.

38. (withdrawn) The electrical device of claim 31, further comprising:

a second strained material formed proximate the strained material and the non-strained material, wherein the strained material is in a tensile or compressive state and the second strained material is in a compressive or tensile state, respectively.

39. (withdrawn) The electrical device of claim 31, wherein the strained material is a carbon doped material or a germanium doped material.

40. (withdrawn) The electrical device of claim 31, further comprising:

a recess formed in the substrate, the recess having side-walls, wherein the strained material is formed within the confines of the sidewalls and is a carbon doped material or a germanium doped material.

41. (withdrawn) The electrical device of claim 40, wherein the sidewalls have an insulating layer and the strained material is formed within the confines of the insulating layer.